UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,857	03/12/2001	Akihiko Koh	SON-2047	3304

23353 7590 09/13/2004

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,857	KOH ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in reply to Applicant's response and amendment filed May 20, 2004. Claims 13-25 are now pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection. It is noted that original claims 1-12 have been canceled and new claims 13-25 have been added.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

It is noted that Figures 1 and 2 are now labeled as "Related Art" in the replacement drawings. However, a legend such as --Prior Art-- is required because only that which is old is illustrated, as indicated in the previous Office action.

Specification

4. The objection to the title of the invention is withdrawn in view of the amendment.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,454,100 to Sagane (art of record) in view of U.S. Pat. No. 5,701,506 to Hosotani (art of record).

With respect to claim 13 (new), Sagane discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program (see column 1, lines 9-14), the data processing apparatus comprising:

(a) a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits (see column 6, line 67 to column 7, line 3, which shows a plurality of correction address registers, i.e. bug address setting registers, and a plurality of comparators, i.e. coincidence detecting circuits),

(i) one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory (see column 6, lines 7-9, which shows a register holding a correction address, and column 3, lines 32-34, which shows that the correction address denotes the start of a buggy part of the program to be corrected),

(ii) one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide (see column 3, lines 48-52, which shows a comparator comparing an execution address, i.e. a program address, with a correction address, i.e. a bug address, and outputting a coincidence signal when the addresses coincide),

(iii) another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory (see column 6, lines 7-9, which shows a register holding a correction address, i.e. another of the plurality of registers holding another correction address, and column 3, lines 32-34, which shows that the correction address denotes the start of a buggy part, i.e. another buggy part, of the program to be corrected),

(iv) another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide (see column 3, lines 48-52, which shows a comparator comparing an execution address with a correction address and outputting a coincidence signal, i.e. another of the plurality of comparators comparing a

program address with a bug address and outputting another coincidence signal, when the addresses coincide); and

(b) a central processing unit receiving said plurality of coincidence signals (see CPU 2 in FIGS. 1 and 3), wherein said central processing unit:

(i) executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses (see column 6, lines 41-52, which shows executing a correction program, i.e. a debugging program, stored within RAM when the addresses coincide),

(ii) executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses (see column 6, lines 41-52, which shows executing a correction program, i.e. another debugging program, stored within RAM when the addresses coincide), and

(iii) executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses (see column 6, lines 37-40, which shows accessing ROM, i.e. executing the program stored within program memory, when there is no coincidence signal).

Although Sagane discloses a plurality of correction address or bug address setting registers and a plurality of comparators or coincidence detecting circuits (see column 6, line 67 to column 7, line 3), and discloses that the comparator, i.e. each comparator, outputs a

coincidence signal (see column 3, lines 48-52), Sagane does not expressly disclose the limitation wherein the central processing unit receives a plurality of coincidence signals.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the plurality of comparators would output a corresponding plurality of coincidence signals to be received by the CPU. Moreover, Hosotani expressly discloses a plurality of changing address registers, i.e. bug address setting registers, and a plurality of match circuits, i.e. coincidence detecting circuits, which output a corresponding plurality of signals (see FIG. 2). Hosotani further discloses that the plurality of comparison signals, i.e. coincidence signals, is received by the CPU for the purpose of correcting a plurality of bugs in the program (see column 4, lines 30-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Sagane with the features taught by Hosotani, so that a program stored in ROM, such as also disclosed by Sagane (see column 1, lines 9-14), can be corrected at a plurality of locations without rebuilding the ROM (see Hosotani, column 1, lines 45-50).

With respect to claim 14 (new), Sagane in view of Hosotani further discloses the limitation wherein an interrupt request for said central processing unit is generated when any of said plurality of coincidence signals indicates a coincidence of said program address and any of said plurality of bug addresses (see Sagane, column 5, lines 13-16, which shows generating an interrupt from the coincidence signal, i.e. any of the coincidence signals, when the corresponding addresses coincide).

With respect to claim 15 (new), Sagane in view of Hosotani further discloses the limitation wherein, when said one of said plurality of coincidence signals indicates said coincidence of said program address and said one of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said one of said plurality of bug addresses to begin execution of said one of a plurality of debugging programs after suspending execution of said program (see Sagane, column 5, lines 17-21, which shows executing a correction program, i.e. a debugging program, at a correction address, i.e. a bug address, after suspending execution),

(c) suspends execution of said one of a plurality of debugging programs by processing an instruction residing within said one of a plurality of debugging programs that has a return address (see Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of a debugging program in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see Sagane, column 5, lines 25-31, which shows returning control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 16 (new), Sagane in view of Hosotani further discloses the limitation wherein, when said another of said plurality of coincidence signals indicates said coincidence of said program address and said another of said plurality of bug addresses, said central processing unit:

(a) suspends execution of said program stored within said program memory after receiving said interrupt request (see Sagane, column 5, lines 11-20, which shows passing control to a correction program in RAM, i.e. suspending execution of the program in ROM, after receiving an interrupt request),

(b) processes an instruction stored within said random access memory at said another of said plurality of bug addresses to begin execution of said another of a plurality of debugging programs after suspending execution of said program (see Sagane, column 5, lines 17-21, which shows executing a correction program at a correction address, i.e. another of the plurality of debugging programs at another of the plurality of bug addresses, after suspending execution),

(c) suspends execution of said another of a plurality of debugging programs by processing an instruction residing within said another of a plurality of debugging programs that has a return address (see Sagane, column 5, lines 22-28, which shows returning to an address in ROM, i.e. suspending execution of another of the plurality of debugging programs in RAM, by processing a jump instruction within the debugging program), and

(d) resumes execution of said program stored within said program memory by processing an instruction residing within said program memory at said return address (see Sagane, column

5, lines 25-31, which shows returning control to the program in ROM, i.e. resuming execution of the program at the return address).

With respect to claim 17 (new), Sagane in view of Hosotani further discloses the limitation wherein said plurality of bug addresses is stored within said random access memory (see Sagane, column 5, lines 44-48, which shows that the correction address, i.e. the bug address, is stored in RAM, and lines 49-54, which shows that there is a plurality of such bug addresses).

With respect to claim 18 (new), Sagane in view of Hosotani further discloses the limitation wherein said plurality of coincidence signals is a plurality of interrupt request signals (see Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows that there is a plurality of such interrupt request signals).

With respect to claim 19 (new), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as separate interrupt requests (see Sagane, column 5, lines 13-16, which shows generating an interrupt request signal from the coincidence signal, and lines 49-54, which shows repeating the interrupt sequence separately for each bug, i.e. such that the CPU receives the plurality of coincidence signals as separate interrupt requests).

With respect to claim 20 (new), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit receives said plurality of coincidence signals as a single interrupt request (see Sagane, column 5, lines 13-16, which shows generating an interrupt

request signal from the coincidence signal, and Hosotani, column 4, line 60 to column 5, line 2, which shows that the CPU receives the plurality of match signals, i.e. coincidence signals, as a single output signal).

With respect to claim 21 (new), Sagane in view of Hosotani does not expressly disclose the limitation wherein said plurality of coincidence signals are logically AND'ed together and input to said central processing unit as an interrupt request signal.

However, Hosotani discloses that the coincidence signals are logically OR'ed together, and that the resulting output is a "1" level when any one of the address comparisons is a match and a "0" level when all of the comparisons are mismatches (see column 4, line 60 to column 5, line 2). In other words, Hosotani defines the coincidence detection circuitry as active high. When the signals are instead defined as active low, the same result is achieved by substituting the OR gate with an AND gate, as is well known in the art. The resulting output from the AND gate, in this case, would then be a "0" level when any one of the address comparisons is a match and a "1" level when all of the comparisons are mismatches.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the logical OR operation disclosed by Hosotani with a logical AND operation when the coincidence detection circuitry is defined as active low, rather than active high as taught by Hosotani, to achieve an equivalent result.

With respect to claim 22 (new), Sagane in view of Hosotani further discloses the limitation wherein said plurality of debugging programs are input during initialization into said random access memory from a source external to said data processing apparatus (see Sagane,

column 3, lines 32-46, which shows inputting the correction content, i.e. the plurality of debugging programs, into RAM from an external EEPROM during initialization).

With respect to claim 23 (new), Sagane in view of Hosotani further discloses the limitation wherein said random access memory stores a plurality of interrupt vectors of start addresses, said start addresses identifying memory areas within said random access memory that contain said plurality of debugging programs (see Sagane, column 5, lines 44-48, which shows that the start address is stored in RAM, and lines 49-54, which shows that there is a plurality of such start addresses that are interrupt vectors corresponding to the locations of a plurality of correction programs, i.e. debugging programs, in RAM).

With respect to claim 24 (new), Sagane in view of Hosotani further discloses the limitation wherein said central processing unit suspends an instruction being executed and reads an instruction code from a program address designated by a predetermined address table when said central processing unit executes any of said plurality of debugging programs stored within random access memory (see Sagane, column 6, lines 41-52, which shows reading instruction data from an address referenced by a predetermined address table and executing a correction program, i.e. any of the plurality of debugging programs, stored in RAM).

With respect to claim 25 (new), Sagane in view of Hosotani further discloses the limitation wherein said program memory is read only memory (see Sagane, column 1, lines 9-14, which shows that the program is stored in ROM).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

After October 25, 2004, the examiner can be reached at (571) 272-3707, and the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3694.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy

ANTONY NGUYEN-BA
PRIMARY EXAMINER